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December 16, 2006

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APPLICATION NUMBER: *10/803,518*
FILING DATE: *March 17, 2004*
RELATED PCT APPLICATION NUMBER: *PCT/US05/06140*

THE COUNTRY CODE AND NUMBER OF YOUR PRIORITY APPLICATION, TO BE USED FOR FILING ABROAD UNDER THE PARIS CONVENTION, IS *US10/803,518*

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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	B-369
First Inventor	Steven C. Taylor
Title	Ultrasonic Pulser-Receiver
Express Mail Label No.	ER202562976US

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

1. [✔] Fee Transmittal Form (e.g., PTO/SB/17) *(Submit an original and a duplicate for fee processing)*
2. [ ] Applicant claims small entity status. See 37 CFR 1.27.
3. [✔] Specification [*Total Pages* 21] *(preferred arrangement set forth below)*
   - Descriptive title of the Invention
   - Cross Reference to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to sequence listing, a table, or a computer program listing appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings *(if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
4. [✔] Drawing(s) *(35 U.S.C. 113)* [*Total Sheets* 4]
5. Oath or Declaration [*Total Pages* 2]
   a. [✔] Newly executed (original or copy)
   b. [ ] Copy from a prior application (37 CFR 1.63 (d)) *(for continuation/divisional with Box 18 completed)*
      i. [ ] DELETION OF INVENTOR(S) Signed statement attached deleting Inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).
6. [ ] Application Data Sheet. See 37 CFR 1.76

ADDRESS TO:

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Washington, DC 20231

7. [ ] CD-ROM or CD-R in duplicate, large table or Computer Program *(Appendix)*
8. Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
   a. [ ] Computer Readable Form (CRF)
   b. Specification Sequence Listing on:
      i. [ ] CD-ROM or CD-R (2 copies); or
      ii. [ ] paper
   c. [ ] Statements verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

9. [✔] Assignment Papers (cover sheet & document(s))
10. [ ] 37 CFR 3.73(b) Statement [ ] Power of Attorney *(when there is an assignee)*
11. [ ] English Translation Document *(if applicable)*
12. [✔] Information Disclosure Statement (IDS)/PTO-1449 [ ] Copies of IDS Citations
13. [ ] Preliminary Amendment
14. [✔] Return Receipt Postcard (MPEP 503) *(Should be specifically itemized)*
15. [ ] Certified Copy of Priority Document(s) *(if foreign priority is claimed)*
16. [ ] Nonpublication Request under 35 U.S.C. 122 (b)(2)(B)(i). Applicant must attach form PTO/SB/35 or its equivalent.
17. [ ] Other: .....

18. If a CONTINUING APPLICATION, *check appropriate box, and supply the requisite information below and in a preliminary amendment, or in an Application Data Sheet under 37 CFR 1.76:*

[ ] Continuation [ ] Divisional [ ] Continuation-in-part (CIP) of prior application No.: ____/____

Prior application information: *Examiner:* _____ *Group Art Unit:* _____

For CONTINUATION OR DIVISIONAL APPS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 5b, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.

19. CORRESPONDENCE ADDRESS

[ ] *Customer Number or Bar Code Label* (Insert Customer No. or Attach bar code label here) or [ ] *Correspondence address below*

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Name (Print/Type)	Alan D. Kirsch	*Registration No. (Attorney/Agent)*	33,720
Signature	Alan D. Kirsch	*Date*	3/17/04

PTO/SB/17 (10-01)
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FEE TRANSMITTAL for FY 2002

Patent fees are subject to annual revision.

TOTAL AMOUNT OF PAYMENT ($) 1184.00

Complete if Known	
Application Number	
Filing Date	
First Named Inventor	Steven C. Taylor
Examiner Name	
Group Art Unit	
Attorney Docket No.	B-369

METHOD OF PAYMENT

1. ☑ The Commissioner is hereby authorized to charge indicated fees and credit any overpayments to:

Deposit Account Number: 05-0565

Deposit Account Name:

☑ Charge Any Additional Fee Required Under 37 CFR 1.16 and 1.17

☐ Applicant claims small entity status. See 37 CFR 1.27

2. ☐ **Payment Enclosed:**

☐ Check ☐ Credit card ☐ Money Order ☐ Other

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
101	740	201	370	Utility filing fee	770.00
106	330	206	165	Design filing fee	
107	510	207	255	Plant filing fee	
108	740	208	370	Reissue filing fee	
114	160	214	80	Provisional filing fee	

SUBTOTAL (1) ($) 770.00

2. EXTRA CLAIM FEES

	Extra Claims		Fee from below	Fee Paid
Total Claims	43 -20** =	23	x 18.00	414.00
Independent Claims	3 - 3** =	0	x 84.00	0.00
Multiple Dependent				

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
103	18	203	9	Claims in excess of 20
102	84	202	42	Independent claims in excess of 3
104	280	204	140	Multiple dependent claim, if not paid
109	84	209	42	** Reissue independent claims over original patent
110	18	210	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) 414.00

**or number previously paid, if greater; For Reissues, see above

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee or oath	
127	50	227	25	Surcharge - late provisional filing fee or cover sheet	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for *ex parte* reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for reply within first month	
116	400	216	200	Extension for reply within second month	
117	920	217	460	Extension for reply within third month	
118	1,440	218	720	Extension for reply within fourth month	
128	1,960	228	980	Extension for reply within fifth month	
119	320	219	160	Notice of Appeal	
120	320	220	160	Filing a brief in support of an appeal	
121	280	221	140	Request for oral hearing	
138	1,510	138	1,510	Petition to institute a public use proceeding	
140	110	240	55	Petition to revive - unavoidable	
141	1,280	241	640	Petition to revive - unintentional	
142	1,280	242	640	Utility issue fee (or reissue)	
143	460	243	230	Design issue fee	
144	620	244	310	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Processing fee under 37 CFR 1.17(q)	
126	180	126	180	Submission of Information Disclosure Stmt	
581	40	581	40	Recording each patent assignment per property (times number of properties)	
148	740	248	370	Filing a submission after final rejection (37 CFR § 1.129(a))	
149	740	249	370	For each additional invention to be examined (37 CFR § 1.129(b))	
179	740	279	370	Request for Continued Examination (RCE)	
169	900	189	900	Request for expedited examination of a design application	

Other fee (specify) _____

*Reduced by Basic Filing Fee Paid SUBTOTAL (3) ($)

SUBMITTED BY				Complete (if applicable)	
Name (Print/Type)	Alan D. Kirsch	Registration No. (Attorney/Agent)	33,720	Telephone	208-526-1371
Signature	Alan D Kirsch			Date	3/17/04

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PATENT APPLICATION
Attorney Docket No. B-369

NOTICE OF EXPRESS MAILING

Express Mail Mailing Label Number: EE202560976US

Date of Deposit with USPS: 3/17/04

Person making Deposit: Mandy Jordan

APPLICATION FOR LETTERS PATENT

FOR

ULTRASONIC PULSER-RECEIVER

INVENTOR:

Steven C. Taylor

From the INTERNATIONAL BUREAU

PCT

NOTIFICATION CONCERNING
SUBMISSION OR TRANSMITTAL
OF PRIORITY DOCUMENT

(PCT Administrative Instructions, Section 411)

To:

KIRSCH, Alan, D.
Battelle Energy Alliance, LLC
P.O. Box 1325
Idaho Falls, ID 83415-3899
ETATS-UNIS D'AMERIQUE

Date of mailing *(day/month/year)* 13 February 2007 (13.02.2007)	
Applicant's or agent's file reference B-369	**IMPORTANT NOTIFICATION**
International application No. PCT/US2005/006140	International filing date *(day/month/year)* 23 February 2005 (23.02.2005)
International publication date *(day/month/year)* **Not yet published**	Priority date *(day/month/year)* 17 March 2004 (17.03.2004)

Applicant
BATTELLE ENERGY ALLIANCE, LLC

1. By means of this Form, which replaces any previously issued notification concerning submission or transmittal of priority documents, the applicant is hereby notified of the date of receipt by the International Bureau of the priority document(s) relating to all earlier application(s) whose priority is claimed. Unless otherwise indicated by the letters "NR", in the right-hand column or by an asterisk appearing next to a date of receipt, the priority document concerned was submitted or transmitted to the International Bureau in compliance with Rule 17.1(a) or (b).

2. *(If applicable)* The **letters "NR"** appearing in the right-hand column denote **a priority document which, on the date of mailing of this Form, had not yet been received by the International Bureau** under Rule 17.1(a) or (b). Where, under Rule 17.1(a), the priority document must be submitted by the applicant to the receiving Office or the International Bureau, but the applicant fails to submit the priority document within the applicable time limit under that Rule, **the attention of the applicant is directed** to Rule 17.1(c) which provides that no designated Office may disregard the priority claim concerned before giving the applicant an opportunity, upon entry into the national phase, to furnish the priority document within a time limit which is reasonable under the circumstances.

3. *(If applicable)***An asterisk (*)** appearing next to a date of receipt, in the right-hand column, denotes **a priority document submitted or transmitted to the International Bureau but not in compliance with Rule** 17.1(a) or (b) (the priority document was received after the time limit prescribed in Rule 17.1(a) or the request to prepare and transmit the priority document was submitted to the receiving Office after the applicable time limit under Rule 17.1(b)). Even though the priority document was not furnished in compliance with Rule 17.1(a) or (b), the International Bureau will nevertheless transmit a copy of the document to the designated Offices, for their consideration. In case such a copy is not accepted by the designated Office as the priority document, Rule 17.1(c) provides that no designated Office may disregard the priority claim concerned before giving the applicant an opportunity, upon entry into the national phase, to furnish the priority document within a time limit which is reasonable under the circumstances.

Priority date	Priority application No.	Country or regional Office or PCT receiving Office	Date of receipt of priority document
17 March 2004 (17.03.2004)	10/803,518	US	22 December 2006 (22.12.2006)

The International Bureau of WIPO 34, chemin des Colombettes 1211 Geneva 20, Switzerland	Authorized officer Nora Lindner
Facsimile No. +41 22 338 82 70	Facsimile No. +41 22 338 82 70 Telephone No. +41 22 338 97 20

Ultrasonic Pulser-Receiver

GOVERNMENT RIGHTS

[0001] This invention was made with Government support under Contract DE-AC07-99ID13727 awarded by the U.S. Department of Energy. The Government has certain rights in the invention.

TECHNICAL FIELD

[0002] The invention relates to data acquisition methods and apparatus. Some aspects of the invention relate more particularly to ultrasonic testing methods and apparatus. Some aspects of the invention relate still more particularly to ultrasonic pulser-receivers.

BACKGROUND OF THE INVENTION

[0003] Ultrasonic testing equipment is used in a variety of applications such as for measuring flow, determining flaws, measuring thickness, and gauging corrosion. This equipment is used with a variety of materials such as metals, plastics, glass, and chemicals. One particular type of ultrasonic testing apparatus is a pulser-receiver. Pulser-receivers are used for a variety of non-destructive testing applications, including flaw detection and thickness gauging. Some pulser-receivers operate at lower frequencies, such as 1/2 MHz to 25 MHz. Certain applications require high frequency pulsers-receivers operating at about 100 MHz.

[0004] Pulser-receivers are available, for example, from GE-Panametrics, 221 Crescent Street, Waltham, MA 02453-3497 USA, such as model number 5058PR, a high

voltage pulser-receiver for ultrasonic test and measurement applications requiring a high material penetration capability; model 5072PR, an ultrasonic pulser-receiver configured to provide high energy, high gain performance for low frequency investigation of attenuating materials; model 5073PR, a broadband 75 MHz ultrasonic pulser-receiver which provides flaw detection capabilities for very high frequency, high resolution ultrasonic testing when used with an oscilloscope and appropriate transducers, model 5077PR, an ultrasonic pulser-receiver for providing high voltage square wave performance over a wide range of applications, model 5800PR, a computer-controlled pulser-receiver for general purpose ultrasonic testing using computer-based systems for automatic testing, or stored setups to speed repetitive manual tasks, and model 5900PR, a computer-controlled pulser-receiver for high frequency ultrasonic testing using computer-based systems for automatic testing, or stored setups to speed repetitive manual tasks.

[0005] Pulser-receivers are also available from JSR Ultrasonics, A Division of Imagilent, 3800 Monroe Avenue, Pittsford, NY 14534 USA, such as model DPR500, which is a dual channel instrument having two pulser-receivers integrated into one unit, and model DPR300, which is a computer controlled ultrasonic pulser-receiver with a low noise receiver.

[0006] For some pulser-receivers, replacement transducers are no longer available. Transducers sometimes fail and require replacement. In some applications, there will be multiple failures per year. The cost of replacement can be, for example, about $10,000 to $16,000. Transducer costs vary based on fabrication yields and availability of parts.

[0007] Another problem with existing transducers is that they are physically large, heavy and focused. These attributes require, in some applications, that transducers be servoed to track the front surface of a sample under inspection. To add a servo sub-system to each of the transducers of a system could be very costly.

[0008] It would be desirable to have, in some embodiments, lower cost pulser-receivers including lower cost transducers. It would also be desirable to avoid the added cost of the transducer servomechanisms, in some embodiments.

[0009] Additionally, the time required for general maintenance (i.e. to replace a failed transducer, align the system, and calibrate the existing transducers) is, for example, 20 to 28 man-days. It would be desirable to provide pulser-receivers, in some embodiments, for which the transducers can be removed and replaced, and the system aligned and calibrated, more quickly.

[0010] In computer-controlled pulser-receivers, a computer will typically send a trigger to a pulser-receiver. The pulser-receiver sends out a high voltage pulse in response to the trigger. A piezoelectric transducer converts electrical energy to mechanical energy and sends out a pulse. When the pulse hits a certain material, such as at an interface of different types of materials, a reflection or echo comes back. There will usually be some ringing.

[0011] It would desirable to have pulser-receivers with quick recovery times, in some embodiments.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

[0013] Fig. 1 is a circuit schematic of receiver circuitry of a pulser-receiver in accordance with various aspects of the invention.

[0014] Fig. 2 is a circuit schematic of pulser circuitry of the pulser-receiver.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0015] This disclosure of the invention is submitted in furtherance of the constitutional purposes of the U.S. Patent Laws "to promote the progress of science and useful arts" (Article 1, Section 8).

[0016] Some aspects of the invention provide high frequency transducers with depth of field, very near front surface resolution, and high sensitivity.

[0017] Some aspects of the invention provide a close coupled pulser-receiver with fast rise and fall time, with gain.

[0018] Some aspects of the invention provide a pulser-receiver of relatively small physical size and that allows for a lightweight search head.

[0019] Some aspects of the invention provide ultrasonic pulser-receiver circuitry, for use with an ultrasonic transducer, the circuitry comprising a circuit board; ultrasonic pulser circuitry supported by the circuit board and configured to be coupled to an ultrasonic transducer and to cause the ultrasonic transducer to emit an ultrasonic output pulse; receiver circuitry supported by the circuit board, coupled to the pulser circuitry, including protection circuitry configured to protect against the ultrasonic pulse and

including amplifier circuitry configured to amplify an echo, received back by the transducer, of the output pulse; and a connector configured to couple the ultrasonic transducer directly to the circuit board, to the pulser circuitry and receiver circuitry, wherein impedance mismatches that would result if the transducer was coupled to the circuit board via a cable can be avoided.

[0020] Figs. 1 and 2 show a pulser-receiver 10 embodying various aspects of the invention. More particularly, Fig. 1 shows receiver circuitry 12 and Fig. 2 shows pulser or transmitter circuitry 14 in accordance with very specific embodiments of the invention. For example, to better enable one of ordinary skill in the art to make and use the invention with undue experimentation, specific component values and integrated circuit part numbers are shown in the figures; however, it will be apparent to those of ordinary skill in the art that similar functionality could be achieved using alternative values or ratios of values or components. The pulser-receiver circuitry is configured to be coupled to a transducer. More particularly, in one embodiment, the pulser-receiver circuitry is configured to be coupled to a model E-1038 ValpeyFisher transducer. Other models could also be used.

[0021] The pulser circuitry 14 and receiver circuitry 12 are mounted on a circuit board 16. In some embodiments, the circuit board 16 is a multi-layer circuit board. More particularly, the circuit board 16 has, in some embodiments, five wiring surfaces or planes. These include a top layer or surface (Fig. 1) upon which is mounted the receiver circuitry 12, a bottom layers or surface (Fig. 2) upon which is mounted the pulser circuitry 14, two ground plane layers (not shown) between the top and bottom layers; the first of which is located directly behind the receiver circuitry layer of Fig. 1 and the

second of which is located behind the pulser circuitry layer of Fig. 2, and a power rail layer (not shown) centered between the pulser and receiver ground planes.

[0022] While other sizes could be used, in some embodiments the circuit board 16 is 0.75" x 2.65" resulting in a compact product. The circuit board 16 is, in turn, enclosed within a watertight housing or enclosure 17 with fittings for a cable connector and a transducer.

[0023] A transducer 18 is connected to an output 20 of the pulser circuitry 14, and to an input 22 of the receiver circuitry 12 via a common connector 24 (J2) on one end 26 of the circuit board 16. The connector 24 mates with an In/Out connector of the transducer 18. A trigger signal to the pulser circuitry 14 and the output signal from the receiver circuitry 12 are obtained at the opposite end 28 of the circuit board via connectors 30 and 32.

[0024] Receiver circuitry 12 shown schematically in Fig. 1 will now be described. The receiver circuitry 12 includes amplifier circuitry 34. More particularly, in the illustrated embodiment, the amplifier circuitry 34 comprises two high-speed current feedback amplifiers, (U-2 and U-3), and their associated feedback resistors. In the illustrated embodiment, amplifiers U-2 and U-3 are defined by OPA658 Burr-Brown integrated circuits; however, other amplifier circuitry could be used, such as circuitry from other manufacturers, other amplifier circuitry designs, or other integrated circuit designations. Feedback resistors R-7, R-8, R-9 are associated with amplifier U-2, and resistors R-11 and R-13 are associated with amplifier U-3.

[0025] The receiver circuitry 12 further includes protection circuitry 36 to protect the amplifier circuitry 34 from the pulser circuitry's output pulse. More particularly, in

the illustrated embodiment, the protection circuitry 36 includes input shunting diodes D-14 and D-15 that protect the input of U-2 from the pulser circuitry's output pulse but do not conduct for the much smaller transducer output signals generated by the transducer 18 from the received signals.

[0026] The receiver circuitry 12 further includes input impedance defining circuitry 37. More particularly, in the illustrated embodiment, the impedance to the receiver circuitry 12 is determined by the sum of the resistance of R-7 and R-8, and equals, in the illustrated embodiment, about 50 Ohms or, more particularly, 52 Ohms in the illustrated embodiment. In some embodiments, a parallel (e.g., 100 Ohm) resistor such as resistor R-6 could be used to define an effective input impedance of 50 Ohms; however, in the illustrated embodiment, resistor R-6 is not loaded or is omitted. The voltage gain of the U-2 amplifier stage is approximately equal to [-R9/(R7 + R8)] = -270/52 $\approx$ -5. This gain is in cascade with the gain of the U-3 stage which is approximately equal to [-R12/R11] = -630/75$\approx$ -8. The receiver's total gain (unterminated) is therefore approximately equal to -5 x -8 = 40. For proper operation the output of the receiver circuitry 12 is terminated in 50 Ohms. This termination causes the output of the receiver circuitry 12 to be attenuated by a factor of two, resulting in a terminated gain of approximately twenty for the illustrated embodiment. In the illustrated embodiment, the total receiver bandwidth is at least approximately 100 MHz. More particularly, in the illustrated embodiment, the receiver bandwidth is above 150 MHz and is close to 200 MHz.

[0027] Circuitry is included to provide positive and negative voltages for the various circuit elements of the receiver circuitry 12. More particularly, in the illustrated

embodiment, voltage regulator circuitry 38 is provided. While other voltages could be used, in the illustrated embodiment, the receiver circuitry 12 receives power from plus and minus five volt rails and the voltage for these rails is generated by plus and minus five volt three terminal regulators U-4 and U-5 respectively. In the illustrated embodiment, the voltage regulator U-4 is defined by an LM78L05 National Semiconductor positive voltage regulator integrated circuit and the voltage regulator U-5 is defined by a LM79L05 negative voltage regulator integrated circuit. These regulators are in turn, powered by +/- 15 VDC supplied to the pulser-receiver 10 from an external power supply (e.g., via a connector J4). The power rails are heavily bypassed at each amplifier.

[0028] In the illustrated embodiment, the receiver circuitry 12 defines a low noise receiver.

[0029] The pulser circuitry 14 is shown schematically in Figure 2. The pulser circuitry includes an input trigger amplifier U-6 (and associated resistors R17 and R18), a trigger driver U-1, transistors Q-1 and Q-2, discharge capacitor C-7, and associated charging and discharging diodes D-5 through D-8. In the illustrated embodiment, the amplifier U-6 is a Burr-Brown OPA658 op-amp; the trigger driver U-1 is a Micrel MIC4422BM integrated circuit; and transistors Q-1 and Q-2 are International Rectifier IRFD310 power MOSFETs; integrated circuits by other manufacturers and other integrated circuits providing similar functionality are possible. Capacitors C-1 and C-2, diode D-1, resistor R-2, and capacitor C-6 define pulse shaping circuitry for the transistors Q-1 and Q-2. Capacitors C-32, C-33, and C-34 are bypass capacitors that filter the incoming voltage.

[0030] The circuitry 14 generates its output pulse through high-speed capacitor discharge. In operation, the circuitry 14 functions as follows:

1. Transistors Q-1 and Q-2 are normally non-conducting which allows capacitor C-7 to charge to approximately 200 VDC through diodes D-5, D-6 and D-7.

2. A trigger pulse received at connector 30 is amplified by U-6 and then applied to the input of the driver U-1.

3. The driver U-1 responds to the trigger by generating a fast positive going large (e.g., 15-volt) pulse at the output of U-1 that is applied to the gates of the transistors Q-1 and Q-2.

4. The gate pulse to Q-1 and Q-2 forces these transistors on at high speed causing C-9 to discharge into the transducer 18 via the diode D-8.

[0031] In the illustrated embodiment, the pulse into the transducer is negative going and has amplitude of approximately 200 VDC. Its fall time is < 1 nanosecond.

[0032] The +/- 5 VDC power rails (50 and 52 in Fig. 2) power the amplifier U-6 of the pulser circuitry 14. The driver U-1 is powered from the external +15 VDC supply. The power rails to U-1 and U-6 are heavily bypassed in the same manner as was done for the receiver circuitry.

[0033] A high power input or power supply (e.g., 200-300 Volts) is provided to the circuitry 14 via a connector J5. Diode D2, D3, and D4 are protection diodes. Resistors R-3 and R-4 are current limiting resistors for the high power input. Capacitors C-11 and C-12 are bypass capacitors for the high power input and help remove noise and ripple from the high power input.

[0034] In some embodiments, some or all of the integrated circuits described above are surface mounted.

[0035] Various pulser-receiver embodiments disclosed herein have a fast rise time of less than 5 nanoseconds or, more particularly, of less than 1 nanosecond. Various pulser-receiver embodiments disclosed herein have a front surface ring down of less than 60 nanoseconds or, more particularly, of less than 40 nanoseconds. Various pulser-receiver embodiments disclosed herein have a transducer delay-line of less than 20 microseconds or, more particularly, none is required. Various pulser-receiver embodiments disclosed herein have a focal length of about 19 microseconds or, more particularly, of exactly 19 microseconds. Various pulser-receiver embodiments disclosed herein have a depth of field, in time, of less than +/- 32 nanoseconds or, more particularly, of +/- 2 microseconds. Various pulser-receiver embodiments disclosed herein have a depth of field, in inches, of less than 0.005 inch or, more particularly, of 0.136 inch.

[0036] Applications for the pulser-receiver include, for example, ultrasonic inspection of materials requiring a depth of field and very near surface resolution. Examples include clad measurements, or flaw inspection such as flaw inspection of nuclear fuel, computer chips, wafers, or other materials.

[0037] In compliance with the statute, the invention has been described in language more or less specific as to structural and methodical features. It is to be understood, however, that the invention is not limited to the specific features shown and described, since the means herein disclosed comprise preferred forms of putting the invention into effect. The invention is, therefore, claimed in any of its forms or

modifications within the proper scope of the appended claims appropriately interpreted in accordance with the doctrine of equivalents.

CLAIMS

What is claimed is:

1. Ultrasonic pulser-receiver circuitry, for use with an ultrasonic transducer, the circuitry comprising:

a circuit board;

ultrasonic pulser circuitry supported by the circuit board and configured to be coupled to an ultrasonic transducer and to cause the ultrasonic transducer to emit an ultrasonic output pulse;

receiver circuitry supported by the circuit board, coupled to the pulser circuitry, including protection circuitry configured to protect against the ultrasonic pulse and including amplifier circuitry configured to amplify an echo, received back by the transducer, of the output pulse; and

a connector configured to couple the ultrasonic transducer directly to the circuit board, to the pulser circuitry and receiver circuitry, wherein impedance mismatches that would result if the transducer was coupled to the circuit board via a cable can be avoided.

2. Ultrasonic pulser-receiver circuitry in accordance with claim 1 and, when in operation, having a rise time of less than 5 nanoseconds.

3. Ultrasonic pulser-receiver circuitry in accordance with claim 1 and, when in operation, having a rise time of less than 1 nanosecond.

4. Ultrasonic pulser-receiver circuitry in accordance with claim 1 and, when in operation with an ultrasonic transducer, having a front surface ring down of less than 60 nanoseconds.

5. Ultrasonic pulser-receiver circuitry in accordance with claim 1 and, when in operation with an ultrasonic transducer, having a front surface ring down of less than 40 nanoseconds.

6. Ultrasonic pulser-receiver circuitry in accordance with claim 1 and, when in operation with an ultrasonic transducer, having a transducer delay-line of less than 20 microseconds.

7. Ultrasonic pulser-receiver circuitry in accordance with claim 1 wherein no transducer delay-line is required.

8. Ultrasonic pulser-receiver circuitry in accordance with claim 1 and, when in operation with an ultrasonic transducer, having a focal length of about 19 microseconds.

9. Ultrasonic pulser-receiver circuitry in accordance with claim 1 and, when in operation with an ultrasonic transducer, having a depth of field, in time, of less than +/- 32 nanoseconds.

10. Ultrasonic pulser-receiver circuitry in accordance with claim 1 and, when in operation with an ultrasonic transducer, having a depth of field, in time, of less than +/- 2 microseconds.

11. Ultrasonic pulser-receiver circuitry in accordance with claim 1 and, when in operation with an ultrasonic transducer, having a depth of field, in inches, of less than 0.005 inch.

12. Ultrasonic pulser-receiver circuitry in accordance with claim 1 and, when in operation with an ultrasonic transducer, having a depth of field, in inches, of less than 0.136 inch.

13. Ultrasonic pulser-receiver circuitry in accordance with claim 1 wherein the circuit board has one side supporting at least a majority of the receiver circuitry and an opposite side supporting at least a majority of the pulser circuitry.

14. Ultrasonic pulser-receiver circuitry in accordance with claim 13 wherein at least a majority of the receiver circuitry is defined by components that are surface mounted onto the circuit board.

15. Ultrasonic pulser-receiver circuitry in accordance with claim 13 wherein at least a majority of the pulser circuitry is defined by components that are surface mounted onto the circuit board.

16. Ultrasonic pulser-receiver circuitry, for use with an ultrasonic transducer, the circuitry comprising:

a circuit board;

ultrasonic pulser circuitry supported by the circuit board and configured to be coupled to an ultrasonic transducer and to cause the ultrasonic transducer to emit an ultrasonic output pulse, the pulser circuitry including an input configured to receive an input pulse from an external source, an input trigger amplifier coupled to the input, a trigger driver coupled to the trigger amplifier, a transistor coupled to the trigger amplifier, and circuitry, including a discharge capacitor and charging and discharging diodes, coupled to the transistor;

receiver circuitry supported by the circuit board, coupled to the pulser circuitry, including protection circuitry configured to protect against the ultrasonic pulse and including amplifier circuitry configured to amplify an echo, received back by the transducer, of the output pulse; and

a connector configured to couple the ultrasonic transducer directly to the circuit board, to the pulser circuitry and receiver circuitry, wherein impedance mismatches that would result if the transducer was coupled to the circuit board via a cable can be avoided.

17. Ultrasonic pulser-receiver circuitry in accordance with claim 16 and, when in operation, having a rise time of less than 5 nanoseconds.

18. Ultrasonic pulser-receiver circuitry in accordance with claim 16 and, when in operation, having a rise time of less than 1 nanosecond.

19. Ultrasonic pulser-receiver circuitry in accordance with claim 16 and, when in operation with an ultrasonic transducer, having a front surface ring down of less than 60 nanoseconds.

20. Ultrasonic pulser-receiver circuitry in accordance with claim 16 and, when in operation with an ultrasonic transducer, having a front surface ring down of less than 40 nanoseconds.

21. Ultrasonic pulser-receiver circuitry in accordance with claim 16 and, when in operation with an ultrasonic transducer, having a transducer delay-line of less than 20 microseconds.

22. Ultrasonic pulser-receiver circuitry in accordance with claim 16 wherein no transducer delay-line is required.

23. Ultrasonic pulser-receiver circuitry in accordance with claim 16 and, when in operation with an ultrasonic transducer, having a focal length of about 19 microseconds.

24. Ultrasonic pulser-receiver circuitry in accordance with claim 16 and, when in operation with an ultrasonic transducer, having a depth of field, in time, of less than +/- 32 nanoseconds.

25. Ultrasonic pulser-receiver circuitry in accordance with claim 16 and, when in operation with an ultrasonic transducer, having a depth of field, in time, of less than +/- 2 microseconds.

26. Ultrasonic pulser-receiver circuitry in accordance with claim 16 and, when in operation with an ultrasonic transducer, having a depth of field, in inches, of less than 0.005 inch.

27. Ultrasonic pulser-receiver circuitry in accordance with claim 16 and, when in operation with an ultrasonic transducer, having a depth of field, in inches, of less than 0.136 inch.

28. Ultrasonic pulser-receiver circuitry in accordance with claim 16 wherein the circuit board has one side supporting at least a majority of the receiver circuitry and an opposite side supporting at least a majority of the pulser circuitry.

29. Ultrasonic pulser-receiver circuitry in accordance with claim 28 wherein at least a majority of the receiver circuitry is defined by components that are surface mounted onto the circuit board.

30. Ultrasonic pulser-receiver circuitry in accordance with claim 28 wherein at least a majority of the pulser circuitry is defined by components that are surface mounted onto the circuit board.

31. An ultrasonic pulser-receiver comprising:

an ultrasonic transducer;

a circuit board;

ultrasonic pulser circuitry supported by the circuit board and coupled to the ultrasonic transducer to selectively cause the ultrasonic transducer to emit an ultrasonic output pulse, the pulser circuitry including an input configured to receive an input pulse from an external computer, input trigger amplifier circuitry coupled to the input, a trigger driver coupled to the input trigger amplifier means, a high power transistor coupled to the trigger amplifier, and a discharge capacitor and charging and discharging diodes coupled to the transistor; and

receiver circuitry supported by the circuit board, coupled to the pulser circuitry, including protection circuitry configured to protect against the ultrasonic pulse and including amplifier circuitry configured to amplify an echo, received back by the transducer, of the output pulse, the ultrasonic pulser-receiver, in operation having a rise time of less than 1 nanosecond.

32. An ultrasonic pulser-receiver in accordance with claim 31 and having, in operation, a front surface ring down of less than 60 nanoseconds.

33. An ultrasonic pulser-receiver in accordance with claim 31 and having, in operation, a front surface ring down of less than 40 nanoseconds.

34. An ultrasonic pulser-receiver in accordance with claim 32 and having, in operation, a transducer delay-line of less than 20 microseconds.

35. An ultrasonic pulser-receiver in accordance with claim 33 wherein no transducer delay-line is required.

36. An ultrasonic pulser-receiver in accordance with claim 34 and, in operation, having a focal length of about 19 microseconds.

37. An ultrasonic pulser-receiver in accordance with claim 35 and, in operation, having a depth of field, in time, of less than +/- 32 nanoseconds.

38. An ultrasonic pulser-receiver in accordance with claim 36 and, in operation, having a depth of field, in time, of less than +/- 2 microseconds.

39. An ultrasonic pulser-receiver in accordance with claim 37 and, in operation, having a depth of field, in inches, of less than 0.005 inch.

40. An ultrasonic pulser-receiver in accordance with claim 38 and, in operation, having a depth of field, in inches, of less than 0.136 inch.

41. An ultrasonic pulser-receiver in accordance with claim 40 wherein the circuit board has one side supporting at least a majority of the receiver circuitry and an opposite side supporting at least a majority of the pulser circuitry.

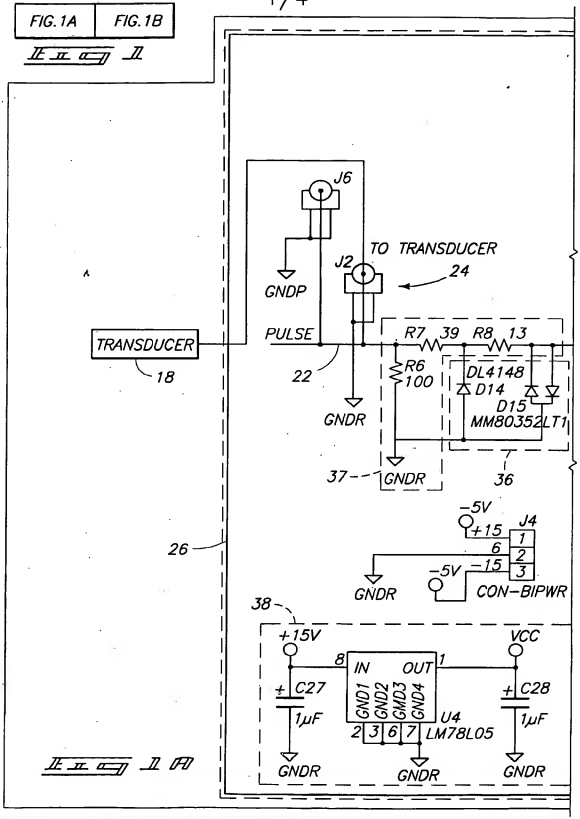
42. An ultrasonic pulser-receiver in accordance with claim 41 wherein at least a majority of the receiver circuitry is defined by components that are surface mounted onto the circuit board.

43. An ultrasonic pulser-receiver in accordance with claim 42 wherein at least a majority of the pulser circuitry is defined by components that are surface mounted onto the circuit board.

ABSTRACT OF THE DISCLOSURE

Ultrasonic pulser-receiver circuitry, for use with an ultrasonic transducer, the circuitry comprising a circuit board; ultrasonic pulser circuitry supported by the circuit board and configured to be coupled to an ultrasonic transducer and to cause the ultrasonic transducer to emit an ultrasonic output pulse; receiver circuitry supported by the circuit board, coupled to the pulser circuitry, including protection circuitry configured to protect against the ultrasonic pulse and including amplifier circuitry configured to amplify an echo, received back by the transducer, of the output pulse; and a connector configured to couple the ultrasonic transducer directly to the circuit board, to the pulser circuitry and receiver circuitry, wherein impedance mismatches that would result if the transducer was coupled to the circuit board via a cable can be avoided.

FIG. 1A | FIG. 1B



Title: Ultrasonic Pulser-Receiver
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B-369

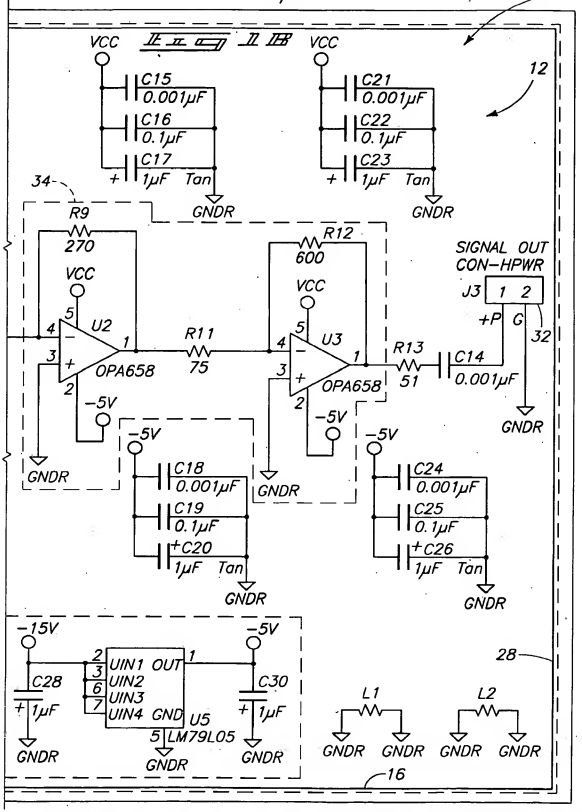

FIG. 2A | FIG. 2B

Fig 2

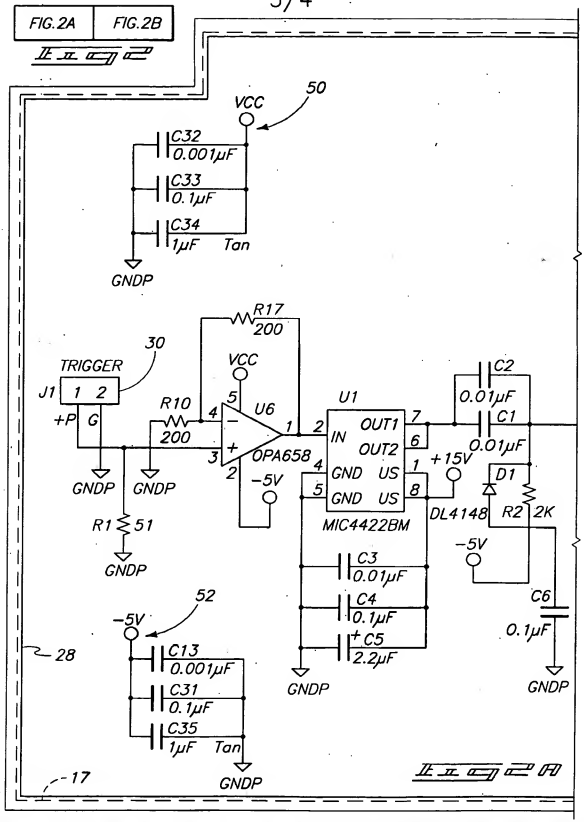

Fig 2A

Title: Ultrasonic Pulser-Receiver
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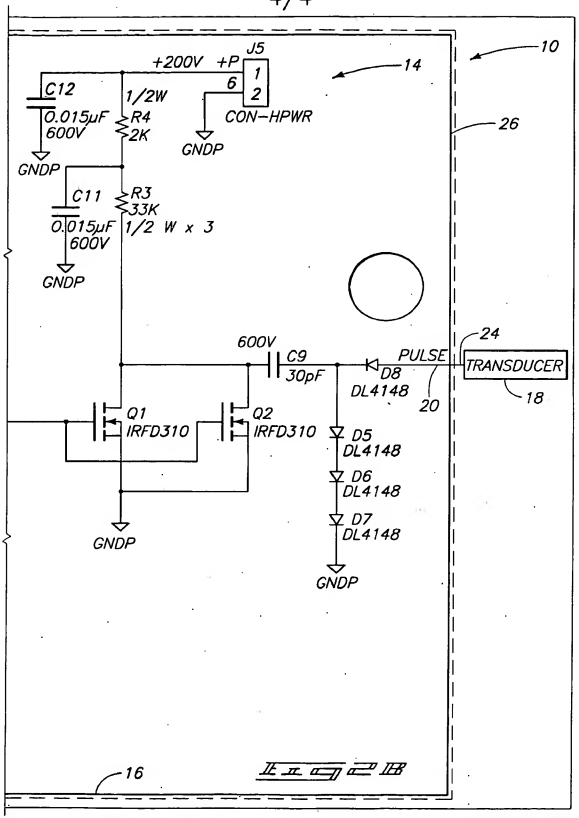

Fig. 1B